Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards

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ABSTRACT

Due to rapid migration to lower power-supply voltages, bus translators are often necessary as an interface between separately powered components of a logic system. This application report is focused on the features of the Texas Instruments AVCA164245 and AVCB164245 (herein referred to as AVCx164245) dual-supply bus-translating transceivers, with some information on other translation parts from the LV1T, LSF, TXB, and TXS families. Each family name here links to a separate application note for additional voltage translation information.

The LV1T family of devices is unique, combining a wide V_{IH} range with a wide V_{CC} range. The LV1T family was created to allow unidirectional up or down voltage translation with only one power rail.

The LSF family of devices consists of passive FET switches that use pullup resistors (external for LSF010x) to allow fast and flexible bidirectional translation between voltage levels.

The TXB push-pull buffered type architecture uses autodirection sensing to remove the requirement for a DIR control signal to establish the direction of data flow. This architecture is designed to exclusively be connected and interfaced with a push-pull CMOS driver and is capable of driving capacitive or high impedance loads in applications such as Secure Digital (SD) or Serial Peripheral Interface (SPI).

The TXS translators also use autodirection sensing and offer system designers a good solution to remedy mixed-voltage system incompatibilities when interfacing with open-drain drivers in applications such as I²C.

The AVC devices provide active buffered bidirectional translation of logic signals between standard power-supply ranges of 3.3 V, 2.5 V, 1.8 V, and 1.5 V. Common problems associated with voltage translation in dual-supply systems are introduced. These problems can be solved by using features of these devices, such as translation, overvoltage tolerance, configurability, input switching levels, bus hold, power-supply isolation, and partial power down.

Keywords: LV1T, LSF, TXB, AVC, AVCA, AVCB, 164245, logic, translation, buffer, overvoltage tolerant, I_{off}, partial power down, 1.5 V, 1.8 V, 2.5 V, 3.3 V, bus hold, configurable

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1   Introduction

Migration to lower power-supply voltages in integrated-circuit logic components and systems is occurring at a faster rate than ever before. This is due, in part, to the increased demand for low-power mobile technologies and the development of advanced small-geometry integrated-circuit (IC) processes to support high-speed applications. Due to this rapid migration, components for these systems often are not available at a single-voltage supply node, and probably will not be for several years, resulting in the need for mixed-voltage designs. Dual-supply bus-translating transceivers provide a solution for interfacing these components, giving the system designer more flexibility in choosing the functionality needed in the design.

The Texas Instruments [AVCA164245](#) and [AVCB164245](#) [1] provide such a solution for translation between logic levels in the 3.3-V, 2.5-V, 1.8-V, and 1.5-V power-supply ranges. These devices are fully configurable for translation between any two of the above logic standards, in either the A-to-B or B-to-A direction. The $\overline{OE}$ and DIR pins are controlled by V_{CCA} on the AVCA device, and by V_{CCB} on the AVCB device. An output driver with slew-rate control provides high dynamic-drive capability, while reducing switching noise. The device supports partial-power-down applications by incorporating overvoltage-tolerant inputs and outputs, power-supply isolation, and powered-down (V_{CC} = 0 V) 3-state mode. Bus-hold options also are available.

2   Interface Problems Without Level Shifting

When interfacing between components using different logic-level standards, two obvious conditions arise:

- A high-voltage device may drive a lower-voltage device.
- A low-voltage device may drive a higher-voltage device.

Each condition presents a unique set of problems that affect proper operation of the system.

2.1   High-Voltage Device Driving a Lower-Voltage Device

High-voltage logic often can reliably drive lower-voltage logic without special translation circuitry as long as two conditions are met:

- The input pins of the receiving device must be specified to be tolerant to the higher voltage.
- The logic swing must pass through the V_{IL} and V_{IH} voltage levels specified for the receiving device.

For example, a 3.3-V device with a CMOS output buffer can drive a 2.5-V device if the latter is overvoltage tolerant because the output rail-to-rail logic swing of 0 V to 3.3 V passes through the 2.5-V device input levels of V_{IL} = 0.7 V and V_{IH} = 1.7 V.

However, several factors might make a receiving device intolerant of a high input voltage:

- The integrated circuit fabrication process may not support the high voltage due to gate-oxide reliability issues (illustrated schematically in Figure 1(a), T_{OX} represents the transistor gate-oxide thickness).
- The input may incorporate an ESD protection diode that provides a current path to V_{CC} (see Figure 1(b)).
- The data input may be a transceiver I/O port that has a parasitic diode to V_{CC}, or output PMOS device that can turn on (see Figure 1(c)). Any of these conditions necessitates the addition of translation circuitry in the interface between the two devices.

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[1]   The AVCA and AVCB versions are referred to collectively as the AVCx164245 throughout the remainder of this application report.

(a) Oxide Integrity   (b) Input ESD Diode   (c) I/O Port Parasitic Diode
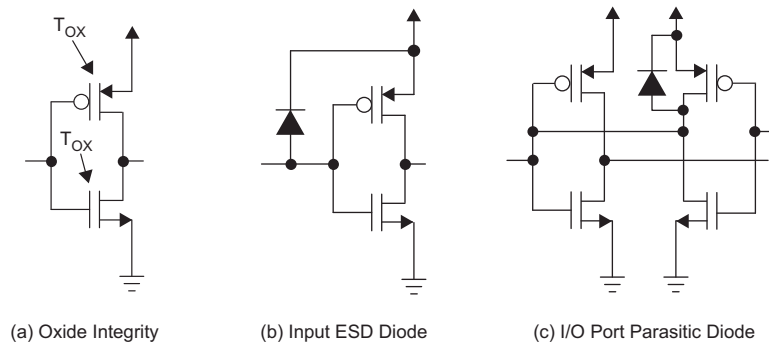
Figure 1. Examples of Circuits That Are Not Overvoltage Tolerant

2.2 Low-Voltage Device Driving a Higher-Voltage Device

Low-voltage logic typically *cannot* drive higher-voltage logic without special translation circuitry. Two problems can occur when attempting to do so. One problem is that, if the voltage difference is large, the low-voltage signal simply does not have enough logic swing to pass through the input V_{IH} level of the receiving device, causing the system to become nonfunctional. For example, in Figure 2(a), a 1.5-V device output driver is shown driving a 3.3-V device input circuit. The logic swing at the input buffer never passes through the required V_{IH} level of 2.0 V, so the input buffer may not switch.

A second problem is that, even if the logic swing is sufficient to switch the receiving device, the V_{IH} level may not be sufficiently high to completely turn off the PMOS device in the input buffer. In the example of Figure 2(b), a logic swing of 2.5 V does exceed V_{IH} of the receiver, so the receiver should switch. However, this condition results in high static power dissipation in the receiver. This is known as the ΔI_{CC} condition. Figure 2(c) shows how a CMOS device supply current increases as its input logic level varies from the V_{CC} or GND rail. The closer the input voltage is to a rail voltage, the lower the ΔI_{CC} current will be. Under normal operating conditions, that is, rail-to-rail swings and fast input edge rates, the device operates outside the high-current region most of the time.
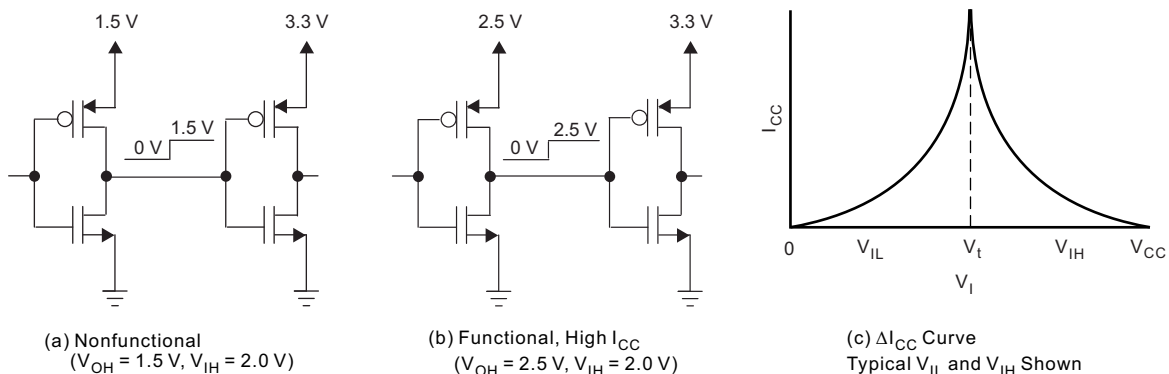

(a) Nonfunctional
(V_{OH} = 1.5 V, V_{IH} = 2.0 V)

(b) Functional, High I_{CC}
(V_{OH} = 2.5 V, V_{IH} = 2.0 V)

(c) ΔI_{CC} Curve
Typical V_{IL} and V_{IH} Shown

Figure 2. Examples of a Low-Voltage Device Driving a Higher-Voltage Device

3 Standard Solutions for Level Shifting and Configurability

Open-collector and open-drain devices offer one solution for voltage translation. The output of such a device can be connected through a pullup resistor to a second power supply. The output V_{OH} is then compatible with the logic levels of the second power-supply system. There are two basic disadvantages to this method:
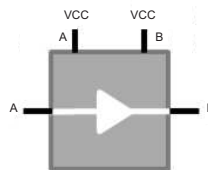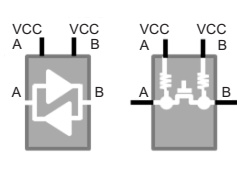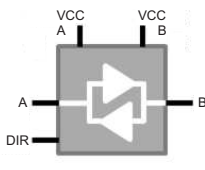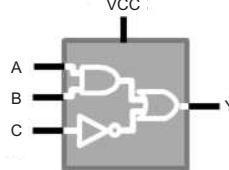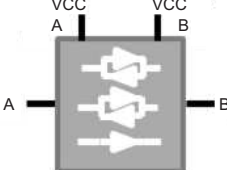
- When the output is low, a constant current flows in the resistor, increasing system power dissipation. A high resistor value is desired to minimize this power.
- The low-to-high signal transition is not an "active" transition, that is, it is determined by the RC time constant of the resistor and the load, and can be slow. A low resistor value is desired to minimize transition time.

Another solution may be FET switches. In addition to their normal use as bus-isolation devices, they can be used for voltage translation in systems where active buffering is not required. TI's CBT, CBTD, and TVC devices offer near-zero propagation delay, with bus-isolation capability. However, they inherently translate only in the downward direction, with a translation difference equal to the threshold voltage of the FET, approximately 1 V. The resulting logic level may or may not be compatible with the desired logic standard, without adjustment, using external components. Unlike an active driver, the FET output impedance becomes very high as the output voltage approaches V_{CC}. This property prevents its use in applications requiring balanced drive. See the CBT application notes listed in the literature section for more details.

To solve these problems, the industry has developed dual-supply voltage-translating buffers and transceivers with active output drivers. These have been most commonly available in 5 V-to-3.3 V and 3.3 V-to-2.5 V versions, although system power-supply voltages are continuing on a downward trend. Many devices on the market are not fully configurable or bidirectional. That is, one V_{CC} and its associated data ports are fixed at the higher power-supply voltage, while the other V_{CC} and associated data ports are fixed at the lower power-supply voltage. Also, many devices may present a current load to the system during partial-power-down applications, and require stringent power-sequencing precautions.

TI has many voltage level translation solutions that cover unidirectional, bidirectional, logic gates, and specific applications. The more popular translation families are summarized in TI's Voltage Level Translation Solutions and the following sections.

TI's Voltage Level Translation Solutions

Unidirectional	Bidirectional	Direction Controlled	Logic	Application Specific
1, 2, 4, 16, 24, 32 bit Push-pull IOs	1, 2, 4, 6, 8, 16, 24, 32 bit Push-pull IOs and Open-drain IOs High frequency support	1, 2, 4, 6, 8, 16, 24, 32 bit Push-pull IOs	Logic input Multiple logic functions	SD Card SIM Card Smart Card IC-USB CF Card Audio Codec
AUP1T, AVC, CD4000, LV-A	GTL, LSF, TXB, TXS	AVC, GTL, LVC	AUP1T, LV1T, LV-A	

3.1 TI's LV1T Solution

The LV1T family of devices is unique, combining a wide V_{IH} range with a wide V_{CC} range. The LV1T family was created to allow up or down voltage translation with only one power rail. The family has overvoltage tolerant inputs that allow down translation from 5.5 V to V_{CC}, which can be as low as 1.65 V. This family has an optimized and balanced output drive of 7 mA at 3.3-V V_{CC}, which reduces line reflection, overshoot and undershoot, and eliminates the need for a damping resistor. Compared to other logic families, the LV1T family is the most well-rounded and universal in terms of specifications. While there are other logic devices with wide-V_{IH} TTL inputs, the LV1T family also has the widest V_{CC} range. The family also has a lowered switching threshold that make it capable of translating signals from as low as 2.1 V up to 5.5 V at V_{CC} = 5 V.

More information on the LV1T family is found in "LV1T Family of Single Supply Translators" (SCEA047).

3.2 TI's LSF Solution

The LSF family of devices consists of passive FET switches that use external pullup resistors to translate between voltage levels. The engineer controls the switching threshold of the device by changing $V_{ref\ A}$. $V_{ref\ B}$ must be ≥0.8 V higher than $V_{ref\ A}$ with a max $V_{ref\ B}$ of 5 V, tied to EN (for LSF010x only), and pulled up to its supply voltage through a 200-kΩ resistor (for LSF010x only). The LSF devices are best suited for translating signals with fast edge rates, and perform well at frequencies up to 200 MHz (down translation) and 100 MHz (up translation). In some special down-translation applications, LSF devices do not require any pullups.

More information on the LSF family is found in "Voltage-Level Translation with the LSF Family," (SLVA675).

3.3 TI's TXB Solution

If a processor GPIO input direction-control signal is not available or if one is not desired, an auto-direction sensing voltage translator can provide a robust solution. As the name implies, this type of translator does not require the use of a direction control signal, and each channel supports independent transmission or reception of data. This eliminates the need for a processor GPIO to control a DIR input, resulting in simplified software driver development as well as smaller device packaging due to reduced pin-count.

The TXB push-pull buffered type architecture does not require a DIR control signal to establish the direction of data flow. This architecture is designed to exclusively be connected and interfaced with a push-pull CMOS driver and is capable of driving capacitive or high impedance loads in applications such as Secure Digital (SD) or Serial Peripheral Interface (SPI). The TXB010x devices are not intended for use in open-drain applications. The TXB translators are fully specified for partial-power-down applications using the I_{off} feature and V_{CC} isolation feature. The TXB devices are suited for translating signals with fast edge rates, and perform well at high data rates up to 100 Mbps.

More information on the TXB family is found in "A Guide to Voltage Translation With TXB-Type Translators," (SCEA043).

3.4 TI's TXS Solution

The TXS translators offer system designers a good solution to remedy mixed-voltage system incompatibilities when interfacing with open-drain drivers in applications such as I^{2}C. These translators eliminate the need for provisioning a GPIO of a processor, since they change the direction of the data flow automatically without the use of a direction control pin. This can simplify software driver development and allows for solutions in smaller packages because of this direction control pin savings.

The TXS (where the "S" indicates switch-type) translators are designed to interface with open-drain drivers and can be used in applications such as I^{2}C. The TXS translators are fully specified for partial-power-down applications using the I_{off} feature and V_{CC} isolation feature.

More information on the TXS family is found in "A Guide to Voltage Translation With TXS-Type Translators," (SCEA044).

3.5 TI's AVCx164245 Solution

The AVCx164245 addresses these constraints by employing a 3.6-V-tolerant process and unique circuitry. The device is designed to translate between logic levels in the 3.3-V, 2.5-V, 1.8-V, and 1.5-V power-supply ranges in either the A-to-B or B-to-A direction. Circuitry is included to simplify bus control and power concerns during power-supply sequencing. Two versions offer control of the $\overline{OE}$ and DIR pins by V_{CCA} logic levels (on the AVCA device), or V_{CCB} logic levels (on the AVCB device).

In addition to translation between two power-supply levels, the AVCx164245 also operates when V_{CCA} and V_{CCB} are equal. Although this is not the target application for a voltage-translating device in a mature single-supply system, it allows more flexibility in selection of components when making board-level revisions and eases the transition between single-supply and dual-supply systems.

3.5.1 AVCx164245 Features and Operation

The AVCx164245 is a 16-bit (dual-octal) noninverting bus transceiver configured as two banks of 8-bit transceivers. Each bank has its own $\overline{OE}$ and DIR for independent control. The device uses two separate configurable power-supply rails (V_{CCA} and V_{CCB}). The A-side I/O port is designed to track V_{CCA}, which accepts any supply voltage from 1.4 V to 3.6 V. The B-side I/O port is designed to track V_{CCB}, and also accepts the 1.4-V to 3.6-V supply-voltage range. Bidirectional level shifting is done internally, and is actively buffered, such that the outputs have full-voltage logic swings on both ports. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The device is designed for asynchronous communication between data buses at different voltage levels. Data is transmitted from the A bus to the B bus, or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input, when low, disables the outputs so the buses are effectively isolated. The data sheet describes the logic function of the $\overline{OE}$ and DIR pins according to the function table (see Table 1).

Table 1. AVCx164245 Function Table (each 8-bit section)

Inputs		Operation
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

3.5.1.1 Input Switching Levels

The AVCx164245 is designed to accommodate power-supply voltages and signal swings in the standard ranges shown in Figure 3. The input switching thresholds, V_T, are designed to linearly track their respective power-supply voltages appropriate to each port, that is, V_T of the A-port and B-port will track V_{CCA} and V_{CCB}, respectively. The device interprets signals above V_{IH} as a logic high and interprets signals below V_{IL} as a logic low. The device can operate throughout the continuous range of 1.4 V to 3.6 V, although it is characterized and specified at only the four standard voltage ranges shown.
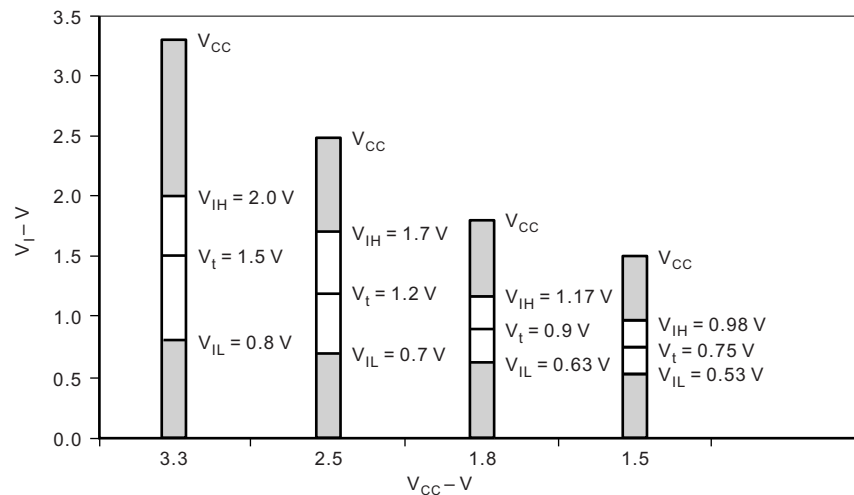
NOTE : Each standard VCC range also has a ± tolerance per the data sheet.

Figure 3. Standard Input Logic Levels Accepted by the AVCx164245

3.5.1.2 Noise Margins

For optimal noise margins, the input voltages to the AVCx164245 should switch rail to rail, which usually is the case for CMOS interfaces. Then, the primary noise-margin concern becomes switching-induced transients, such as ringing, undershoot, overshoot, or transmission-line reflections. This noise should not fall into the voltage range from V_{IL} to V_{IH} specified for the chosen switching standard, otherwise data corruption may result. From Figure 3, the logic-high noise margin is $V_{CC} - V_{IH}$, and the logic-low noise margin is $V_{IL} - GND$. If the driving device is dc terminated, the V_{CC} and GND voltages in these expressions should be substituted by using V_{OH} and V_{OL} levels per the data sheet, determined by the dc drive current, resulting in reduced noise margin.

Because the A-port and B-port thresholds track their respective V_{CC} voltages, determination of noise margin is straightforward. However, because the $\overline{OE}$ and DIR pins may be driven from either V_{CCA} or V_{CCB} logic levels (see *Section 3.5.1.3*), care must be taken to observe the proper noise margin based on the device type chosen (AVCA or AVCB).

3.5.1.3 Configurability

In general, the AVCA device should be chosen if the $\overline{OE}$ and DIR control signals are referenced to V_{CCA}, or the AVCB device should be chosen for V_{CCB}-referenced control signals. However, the configurability of the OE and DIR pins can be enhanced for future system modification by choosing the device version that matches the *lowest voltage* power supply of the system. For example, if V_{CCA} is lowest, choose the AVCA device. If V_{CCB} is lowest, choose AVCB. Due to the overvoltage tolerance of the input pins, this allows the $\overline{OE}$ and DIR inputs to be driven from either V_{CCA} or V_{CCB} logic levels if a system revision requires it.

This down-translation feature of the control inputs is an advantage offered by any overvoltage-tolerant device. Overdriving these inputs does not cause a problem, and the device functions properly, as long as rail-to-rail logic swings, with adequate noise margins, are applied. The system designer then is free to apply either a V_{CCA}- or V_{CCB}-referenced signal level without causing the interface problems discussed previously. This may eliminate the need to include additional control-signal translation hardware in the system. The configurability offered by these two devices, plus the symmetrical bidirectional properties of the translators, offer greater flexibility in PC board routing, component selection and placement, and voltage-supply migration, resulting in overall savings in system costs.

3.5.1.4   Switching Waveforms

Examples of switching waveforms during translation in the A-to-B direction are shown in Figure 4 and Figure 5. Waveforms in the B-to-A direction look identical because device operation is symmetrical. Logic levels at the extreme limits were chosen to better illustrate the translation feature. Industry standards define a different test load for each power-supply range, and are specified in the data sheet. Buffering from A (3.6 V) to B (3.6 V), with the standard test load of 500 Ω and 50 pF, is shown in Figure 4(a), while translation from A (3.6 V) to B (1.4 V), with the standard test load of 2 kΩ and 15 pF, is shown in Figure 4(b).

Translation from A (1.4 V) to B (3.6 V), with the standard test load of 500 Ω and 50 pF, is shown in Figure 5(a), while buffering from A (1.4 V) to B (1.4 V), with the standard test load of 2 kΩ and 15 pF, is shown in Figure 5(b).

(a) V_{CCB} = 3.6 V   (b) V_{CCB} = 1.4 V
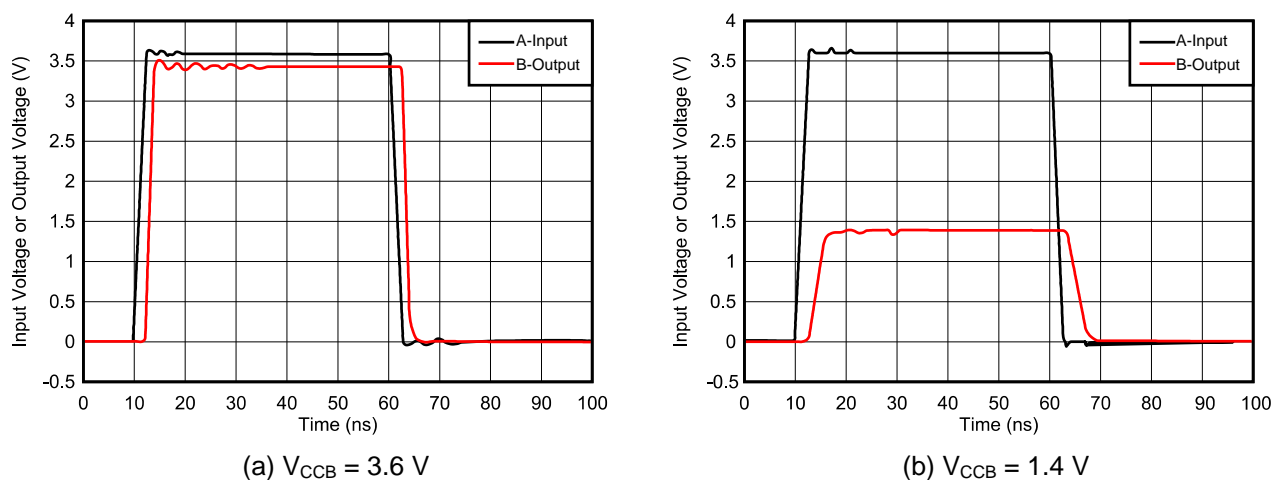
Figure 4. A-to-B Switching Waveforms With V_{CCA} (Input) = 3.6 V

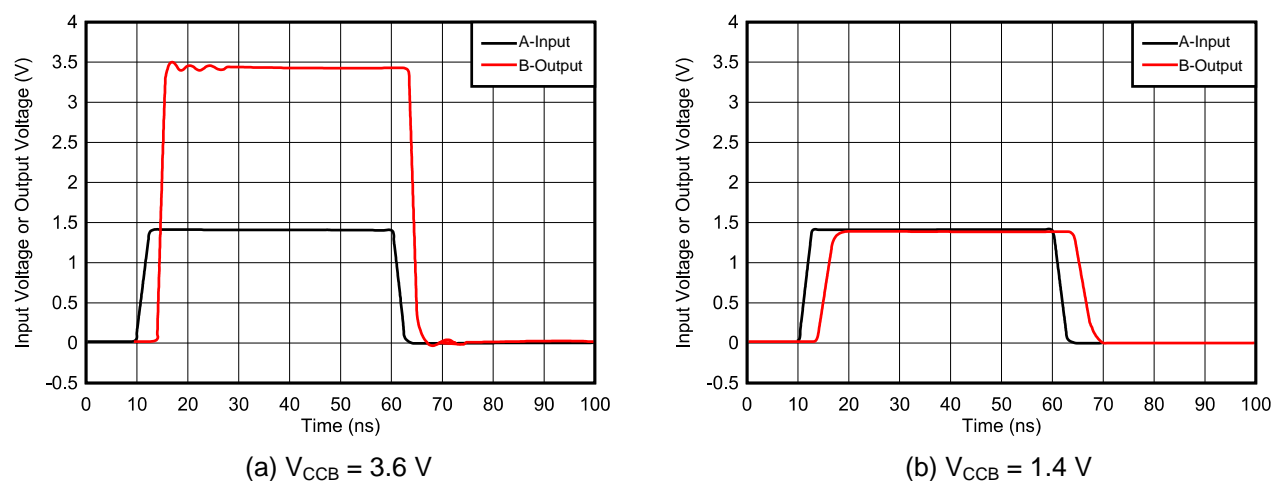(a) V_{CCB} = 3.6 V   (b) V_{CCB} = 1.4 V

Figure 5. A-to-B Switching Waveforms with V_{CCA} (Input) = 1.4

3.5.1.5   Propagation Delays at Different Supply Voltages

As with any CMOS logic device, propagation delay is affected by the power-supply voltage (VCC). The AVCx164245 is optimized for a 1.8-V to 3.3-V translation, where t_{pd} is specified at 4.3 ns max, and for a 2.5-V to 3.3-V translation, where t_{pd} is specified at 3.4 ns max. Other combinations throughout the 1.4-V to 3.6-V range were characterized to determine data-sheet limits. Generally, the lower the V_{CC}, the slower a CMOS device switches. In a voltage translator, an additional effect, related to the *difference in magnitude* between the two supply voltages can occur. Figure 6 illustrates this effect.

Figure 6(a) shows that the A-to-B t_{pd}, when V_{CCB} = 3.0 V actually becomes slower than that at V_{CCB} = 2.3 V as V_{CCA} is lowered to 1.4 V, because the V_{CC} difference is greater. Figure 6(b) shows a similar effect on the V_{CCB} = 1.4 V curve for the B-to-A direction. These plots show simulated worst-case propagation delays at 85°C and weak-process conditions. A constant 15-pF, 2-kΩ load was used in this analysis to observe the V_{CC} dependence, keeping all other factors constant. Due to the difference in test load, these results may not agree with the data-sheet limits. Consult the data sheet for parameter values at specified test conditions.

(a) t_{pd} vs V_{CCA} and V_{CCB} (A to B)

(b) t_{pd} vs V_{CCA} and V_{CCB} (B to A)
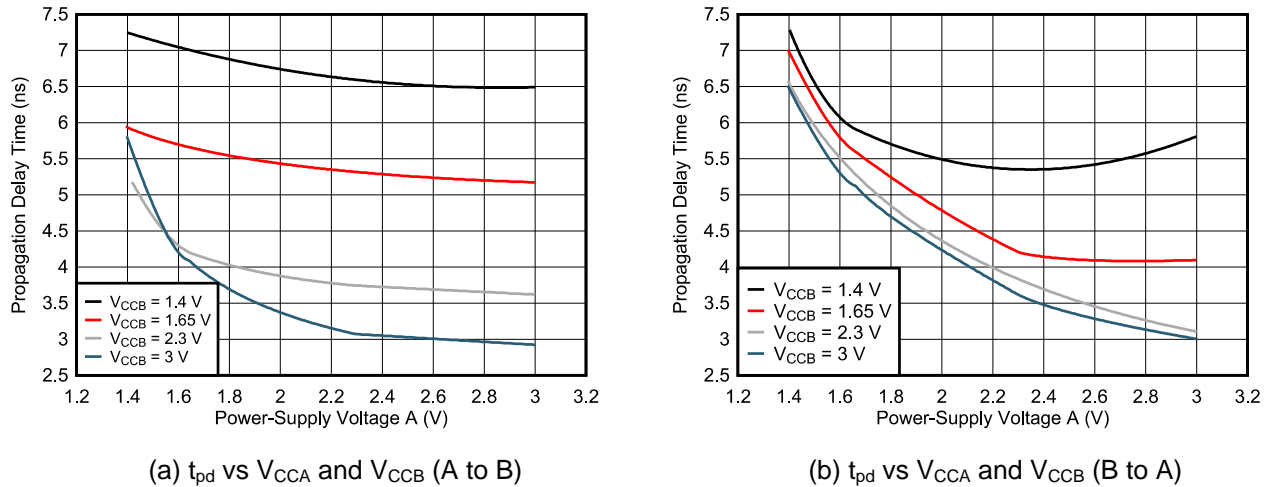
Figure 6. Propagation Delays vs V_{CCA} and V_{CCB}

3.5.1.6 *Output Circuit With Slew-Rate Control*

The AVCx164245 employs a unique output driver common to other members of TI''s AVC logic family. During a signal transition (see Figure 7), this circuit initially lowers the slew rate to reduce switching noise, then lowers the output impedance to provide high-current drive and, finally, near the end of the transition, raises the impedance to limit the overshoot and undershoot noise inherent in high-speed, high-current devices. This allows a single device to have characteristics similar to series-damping-resistor outputs during static conditions, and similar to high-current outputs during dynamic conditions, eliminating the need for series-damping resistors. Due to the unique characteristics of this output, the dc drive-current specifications, I_{OL} and I_{OH}, are not useable as a relative indicator of the dynamic performance. However, the dynamic drive capability is equivalent to standard outputs with I_{OL} and I_{OH} of ±24 mA at 2.5-V V_{CC}.
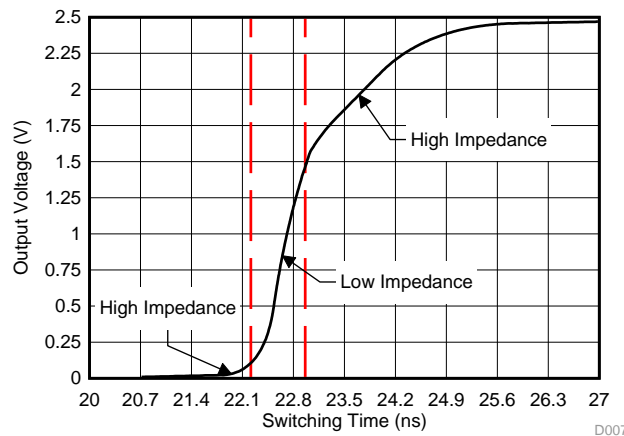
Figure 7. Typical AVCx164245 Output Switching Waveform

3.5.1.7   Power Dissipation

Two data-sheet parameters are used to calculate power dissipation: I_{CC} – for static (nonswitching) power and C_{pd} – for dynamic (switching) power. Both of these parameters are specified separately for each of the two power supplies. A calculation of the total power dissipation of the device should include the effects of both power-supply currents, as well as load currents, if applicable.

3.5.1.7.1   Static Power

The static current of CMOS devices typically is a result of only the reverse-biased junction leakages within the integrated circuit. As a result, these devices have very low static-power dissipation. The AVCx164245 includes a low-power bias circuit that enables its unique partial-power-down features, but adds a small amount of I_{CC}. Even so, the data-sheet I_{CC} maximum limit for each supply at 3.6 V is a low 40 µA and lower than that for reduced V_{CC} levels. The maximum total static power dissipation at 3.6 V can be calculated as:

$$P_{TOTAL} = (I_{CCA})(V_{CCA}) + (I_{CCB})(V_{CCB}) = (40 \text{ µA})(3.6 \text{ V}) + (40 \text{ µA})(3.6 \text{ V}) = 288 \text{ µW}$$

Because the A-port circuitry is isolated and independent of the B-port circuitry, this calculation can be performed in the same manner for all specified combinations of V_{CC}. Note that I_{CC} is specified with no dc load. If a dc load is applied, additional power dissipation may occur in each output driver due to I_{OL} or I_{OH} current (in active mode), or I_{OZ} or I_{off} leakage (in high-impedance mode, typically negligible). In active mode, the power calculation is:

$$P_{TOTAL} = (I_{CCA})(V_{CCA}) + (I_{CCB})(V_{CCB}) + (I_{OL})(V_{OL})(N_L) + (I_{OH})(V_{CC} - V_{OH})(N_H)$$

Where:

N_L = number of outputs low
N_H = number of outputs high
V_{CC} = supply voltage of driver port

3.5.1.7.2   Dynamic Power

The dynamic current of a CMOS device is the result of switching transients within the device. Several factors specific to a given application contribute to dynamic power dissipation, such as V_{CC}, frequency, number of outputs switching, and load. The power-dissipation capacitance parameters, C_{pdA} and C_{pdB}, are provided on the data sheet as a convenient method for calculation of dynamic power dissipation, considering all the above factors. As an example, consider an AVCx164245 operating in the A-to-B direction with V_{CCA} = 3.6 V, V_{CCB} = 2.5 V, frequency = 20 MHz, and one-half of the 16 outputs switching into a 30-pF load. Note that one-half of the outputs switching is a generally recognized principle for calculating typical power consumption over an extended period of time with random data patterns.

$$P_{total} = P_{device} + P_{load}$$

$$P_{device} = [(C_{PDA} \times V_{CCA}^2) + (C_{PDB} \times V_{CCB}^2)] \times f \times N_{sw}$$

$$= [(14 \text{ pF})(3.6 \text{ V})^2 + (20 \text{ pF})(2.5 \text{ V})^2](20 \text{ MHz})(8) = 49 \text{ mW}$$

$$P_{load} = C_L \times V_{CCB}^2 \times f \times N_{sw} = (30 \text{ pF})(2.5 \text{ V})^2(20 \text{ MHz})(8) = 30 \text{ mW}$$

$$P_{total} = 49 \text{ mW} + 30 \text{ mW} = 79 \text{ mW}$$

C_{pd} is specified in the data sheet at 3.3 V only. However, for the recommended operating range of V_{CC} for this device, C_{pd} is proportional to V_{CC}, and so can be extrapolated for other voltage ranges. The total power dissipation also includes the static component, but in this case, as for most CMOS devices, it is negligible compared to the dynamic component. For more details, see the TI application note *CMOS Power Consumption and CPD Calculation*, (SCAA035B).

3.5.1.8 Partial Power-Down Applications

In multiple power-supply systems, a major concern is the behavior of the various parts of the system as the voltage supplies are powered up or powered down. The power-up/power-down sequence can cause some components to be active while others are in power-down mode. This can affect data integrity, power dissipation, and reliability of system components. To avoid these problems, devices operating from different supplies must not present a current load to the system when they are powered down, and their input and output ports must present a high impedance to the bus. That is, the device must block current flow from the I/O ports to V_{CC} or GND. The AVCx164245 is fully specified for partial-power-down applications using the parameters I_{OZ}, I_{off}, and I_{CC}.

3.5.1.8.1 Power-Down 3-State and I_{off}

The AVCx164245 is designed such that, if one V_{CC} is at 0 V while the other V_{CC} remains active, the powered port will be in the high-impedance state, regardless of the state of the $\overline{OE}$ or DIR pins. When a port is in the high-impedance state, whether controlled by the $\overline{OE}$ or DIR pin, or by a partial-power-down V_{CC} level, that port can be driven by voltages higher than V_{CCA} or V_{CCB}, up to 3.6 V (recommended 4.6-V absolute maximum). This is made possible by the I_{off} circuitry, which disables the outputs, preventing damaging reverse current through the upper output transistor and its parasitic diode when it is powered down. The I_{OZ} and I_{off} parameters in the data sheet (see Table 2) specify the maximum leakage to be less than 12.5 µA into the high-impedance port under these disabled conditions.

3.5.1.8.2 Floating Inputs and V_{CC} Pins

In general, input pins of logic devices should not be left open or floating, with no applied voltage bias. However, the AVCx164245 is designed to allow data ports to float as long as their associated V_{CC} pins also are floating, that is, not connected to any power supply or other source of current. This causes the other (powered) port to go into the high-impedance state, regardless of the state of the $\overline{OE}$ or DIR control pins. This feature is useful in applications where a circuit board or cable may need to be left disconnected from a socket providing power. The floating ports are disabled so that high power dissipation and/or oscillations typically associated with CMOS floating inputs do not occur. However, the powered ports should continue to be driven by valid logic levels to prevent similar problems on those ports.

3.5.1.8.3 Voltage-Supply Isolation

The two power supplies of the AVCx164245 are isolated electrically from each other, which means that practically no current will flow between the V_{CCA} and V_{CCB} pins under recommended operating conditions, including partial power down. This is specified in the data sheet as a subset of the I_{CC} parameter (see Table 2). The current of the V_{CC} supply that is powered up is specified as a positive 40-µA maximum (at 3.6 V), and accounts for internal leakage and bias currents. The current of the V_{CC} supply that is powered down (0 V) is specified as a negative 10 µA to account for internal leakage between supplies. Note that, by convention, positive current is into the pin, and negative current is out of the pin.

Table 2. Parameters That Specify Partial-Power-Down Mode Device Currents

Parameter		Test Conditions	V_{CCA}	V_{CCB}	MIN	MAX	Unit
I_{OZ}	A or B ports	$V_O = V_{CCO}$ or GND, $V_I = V_{IH}$ or V_{IL}, $\overline{OE} = V_{IH}$	3.6 V	3.6 V		±12.5	µA
	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{IH}$ or V_{IL}, $\overline{OE} = V_{IH}$ or V_{IL}	0 V	3.6 V		±12.5	
	A port		3.6 V	0 V		±12.5	
I_{off}	A port	V_I or V_O = 0 to 3.6 V	0 V	0 to 3.6 V		±10	µA
	B port		0 to 3.6 V	0 V		±10	
I_{CCA}		$V_I = V_{CCI}$ or GND, $I_O = 0$	0V	3.6 V		−10	µA
			3.6 V	0 V		40	
I_{CCB}		$V_I = V_{CCI}$ or GND, $I_O = 0$	0 V	3.6 V		40	µA
			3.6 v	0 v		−10	

Figure 8 graphically depicts I_{CC} and I/O port states during the partial-power-down conditions mentioned previously. Figure 8(a) shows the normal operating mode with both V_{CC} supplies powered up. Assuming that $\overline{OE}$ and DIR are selecting the A-to-B mode, the A port is configured as an input, and the B-port is an output. Both V_{CC} pins sink I_{CC} current per the data-sheet specification. Figure 8(b) and Figure 8(c) show what happens when one V_{CC} is powered down (V_{CC} = 0 V). All output drivers are disabled into the high-impedance state. The inputs referenced to the 0-V supply are disabled. The inputs referenced to the powered-up side are enabled and, as such, should be biased with valid logic signals to avoid high ΔI_{CC} currents or oscillations. Figure 8(d) shows that when both power supplies are powered down, all inputs and outputs are disabled in the high-impedance state.
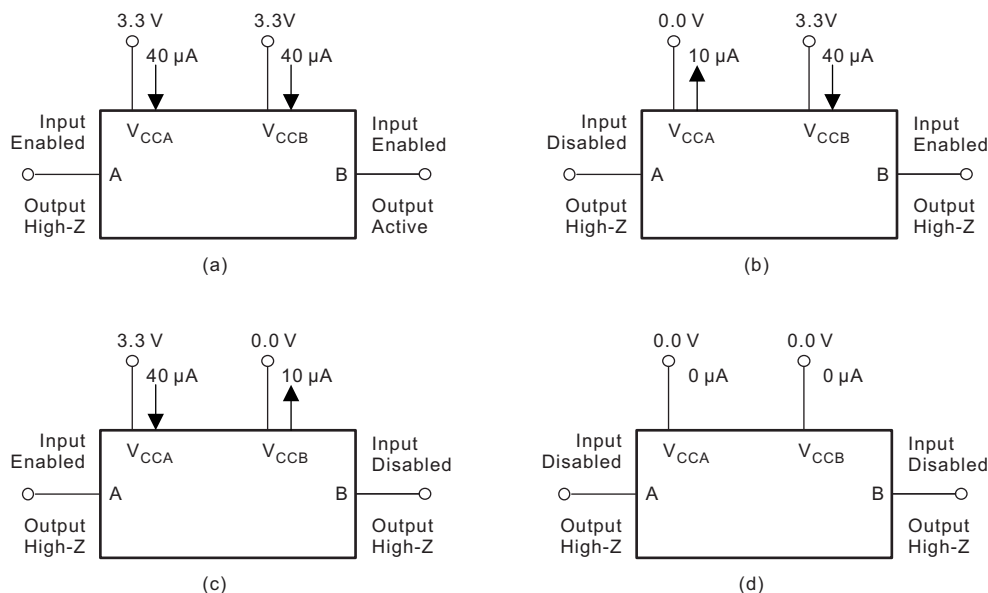
**Figure 8. Graphical Depiction of I_{CC} and I/O Port States
for Partial-Power-Down Conditions (A-to-B Mode)**

3.5.1.8.4   *Power-Up/Power-Down Sequencing Precautions*

The AVCx164245 is quite tolerant of power-supply sequencing. However, a few precautions should be observed to ensure that bus contention, excessive currents, or oscillations do not occur:

1. Connect ground before any supply voltage is applied.
2. Either V_{CC} can be powered up first. Inputs associated with that V_{CC} should receive valid logic levels. The other V_{CC}, at 0 V, causes all outputs to be in the high-impedance state.
3. DIR should ramp with V_{CCA} (AVCA) or V_{CCB} (AVCB), or the highest of the two (see the Configurability section) for A-to-B mode, or should be at ground for B-to-A mode.
4. Power up the second V_{CC}. A pullup resistor from $\overline{OE}$ to V_{CCA} (AVCA) or V_{CCB} (AVCB) ensures that both ports remain in the high-impedance state. The minimum value of the resistor is determined by the current-sinking capability of the driver.
5. Reverse the above sequence for a power-down operation.

Typical laboratory data of partial-power-down supply currents versus a ramping V_{CC} is shown in Figure 9. The device was in A-to-B mode, DIR tied to V_{CCA}, $\overline{OE}$ grounded, and no dc load on the outputs. As expected, I_{CC} of the ramping supply increases with supply voltage. I_{CC} of the steady supply remains fairly constant, with the exception of a small spike below the recommended operating conditions, where the power-down 3-state circuit deactivates.
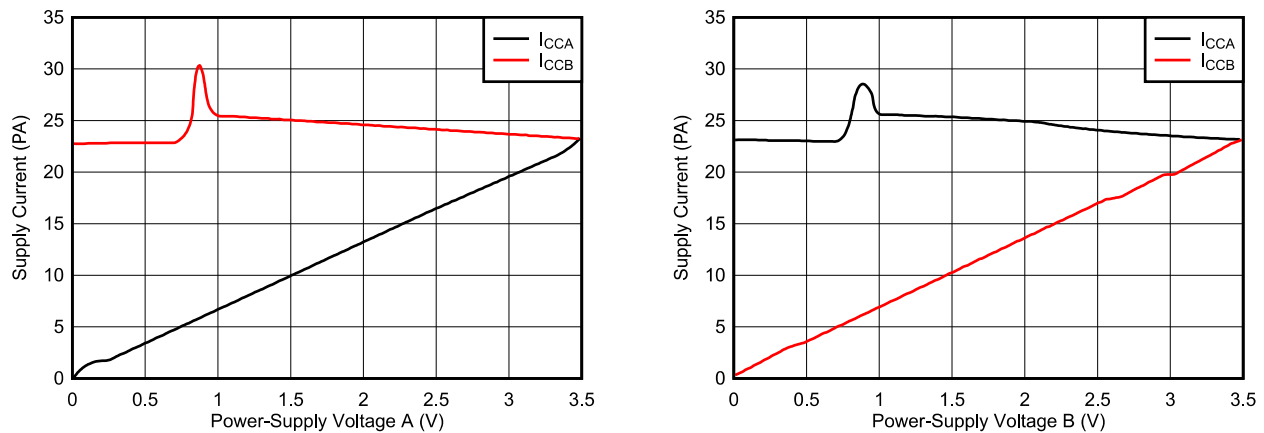
Figure 9. Partial-Power-Down Supply Current (I_{CC}) vs V_{CC}

3.6   Bus-Hold Options

The AVCx164245 also is available in a bus-hold version, designated as the AVCxH164245. Bus hold essentially is a weak latch integrated into each I/O port to prevent floating inputs. In the input schematic of Figure 10, transistors Q3 and Q4 form the bus-hold drivers for the input inverter composed of transistors Q1 and Q2. Diode D2 is added to prevent current flow through parasitic diode D3 and transistor Q3 during overvoltage or partial-power-down events. This circuit will hold an attached bus in its previous logic state if the bus is not driven by another device. This prevents the voltage on the high-impedance bus from drifting to an intermediate state between logic 0 and logic 1, which could lead to oscillations and high power dissipation in devices attached to the bus.

The AVCxH164245, with bus hold, is more robust for partial-power-down applications because it holds the enabled inputs at a valid logic level until another device takes control of the bus. Integrated bus hold eliminates the need for external pullup/pulldown resistors on the I/O ports. In fact, resistors are not recommended because they may form a voltage divider with the bus-hold circuit, presenting an invalid logic state on the bus. For a detailed description of the bus-hold feature, see TI application report *Bus-Hold Circuit*, (SCLA015).
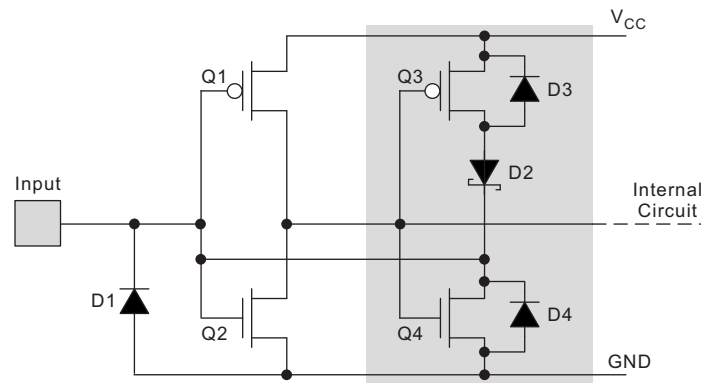
Figure 10. Bus-Hold Circuit

3.7   Package Options

The AVCx164245 pin layout was designed to be compatible with other standard SN74xxx16245 devices, further easing the transition from single-power-supply to dual-power-supply systems. The V_{CCA} and V_{CCB} pins simply can be connected together for single-supply applications. The flow-through data path simplifies printed-circuit-board layout, and the distributed power and ground pins help minimize switching noise. The device is available in the packages shown in Table 3.

Table 3. Package Options

Pins	Description	TI Designator	Lead Pitch (mm)	Dimensions (mm)
48	TSSOP	DGG	0.50	12.6 × 8.3
48	TVSOP	DGV	0.40	9.8 × 6.6
56	VFBGA	GQL	0.65	7.1 × 4.6

4   Conclusion

Common problems associated with voltage translation in dual-supply logic systems, with V_{CC} ranging from 1.4 V to 3.6 V, can be solved by incorporating TI's voltage translation parts from the LV1T, LSF, and TXB families or the AVCA(B)164245 or AVCA(B)H164245 dual-supply bus-translating transceivers in the logic interface. These devices are configurable, symmetrical, and bidirectional, to drive full-rail logic signals on both ports, and include features that enable robust partial-power-down applications.

The AVCx164245 devices are members of the Texas Instruments Widebus™ family. TI's advanced 0.5-micron Enhanced-Performance Implanted CMOS (EPIC™) fabrication process is used to produce the devices.

5   Glossary

AVC	Advanced very-low-voltage CMOS family
AVCA	AVC translator with control inputs referenced to V_{CCA}
AVCB	AVC translator with control inputs referenced to V_{CCB}
CBT	Cross-bar technology (family of FET switches)
CBTD	Cross-bar technology with integrated diode
DMOS	Complementary metal oxide semiconductor (process for fabricating integrated circuits).
ΔI_{CC}	The difference in power-supply current when a CMOS input pin is biased at a voltage less than full rail versus biased at full rail
ESD	Electrostatic discharge
FET	Field-effect transistor
I_{CC}	Power-supply current (from V_{CC})
I_{off}	The maximum leakage current into or out of an input or output port when biased to a specified voltage while V_{CC} = 0 V
I_{OH}	High-level output current
I_{OL}	Low-level output current
LVTTL	Low-voltage transistor-transistor logic
Noise margin	For logic low (high) signals, the difference between the signal amplitude, including noise, and the V_{IL} (V_{IH}) specification of the receiving device
Overvoltage tolerant	The capability of a device input pin or output pin to be subjected to a voltage higher than its power-supply voltage without being damaged
TSSOP	Thin shrink small-outline package
TVC	Translation voltage clamp (family of FET switches)
TVSOP	Thin very small-outline package
V_{CC}	Power-supply voltage (sometimes referred to as V_{DD})
VFBGA	Very-thin fine-pitch ball grid array (package)
V_{IH}	High-level input voltage, above which a logic high is defined
V_{IL}	Low-level input voltage, below which a logic low is defined
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_T	Threshold voltage

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6   Texas Instruments Literature

1. *Texas Instruments Voltage-Level-Translation Devices* (SCEA021)
2. *Benefits and Issues on Migration of 5-V and 3.3-V Logic to Lower-Voltage Supplies* (SDAA011A).
3. *Implications of Slow or Floating CMOS Inputs* (SCBA004C).
4. *Bus-Hold Circuit* (SCLA015)
5. *Flexible Voltage-Level Translation With CBT Family Devices* (SCDA006)
6. *5-V to 3.3-V Translation With the SN74CBTD3384* (SCDA003B).
7. *3.3-V to 2.5-V Translation with Texas Instruments Crossbar Technology* (SCDA004A)

Revision History

Changes from A Revision (July 2004) to B Revision   **Page**

- Changed document title. ………………………………………………………………………………………………… 1
- Added text in the Abstract highlighting the LV1T and LSF device families, TXB architecture, TXS translators, and the AVC devices.…… 1
- Added information the*TI's Voltage Level Translation Solutions* table. ……………………………………………………… 5

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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